CHAPTER 4
Z86017 / Z16017
CONFIGURATION REGISTERS

4.1 INTRODUCTION

Support for the PCMCIA Configuration Registers is provided by the 017. The Register decodes are shown in Table 4-1.

Three additional registers have been added to the 017 to provide an EEPROM link to support remote programming for attribute memory.

Table 4-1. PCMCIA Address xx0H to xx8H, Configuration Register Decode

/WE	/OE	/REG	/CE1	/CE2	Address	Action
1	0	0	0	1	xx0Hx	Read Configuration Option Register
0	1	0	0	1	xx0Hx	Write Configuration Option Register
1	0	0	0	1	xx2Hx	Read Card Configuration and Status
0	1	0	0	1	xx2Hx	Write Card Configuration and Status
1	0	0	0	1	xx4Hx	Read Pin Replacement Register
0	1	0	0	1	xx4Hx	Write Pin Replacement register
1	0	0	0	1	xx6Hx	Read Socket and Copy Register
0	1	0	0	1	xx6Hx	Write Socket and Copy Register
1	0	0	0	1	xx8Hx	Read I/O Event Indication Status*
0	1	0	0	1	xx8Hx	Write I/O Event Indication Status*

Table 4-2. Zilog EEPROM Programming Extensions

/WE	/OE	/REG	/CE1	/CE2	Address	Action
0	1	0	0	1	7F0H	Write EEPROM Address
1	0	0	0	1	7F0H	Read EEPROM Status
0	1	0	0	1	7F2H	Write EEPROM Data
1	0	0	0	1	7F2H	Read EEPROM Data
0	1	0	0	1	7F4H	EEPROM Command
1	0	0	0	1	7F6H	Revision Register

Note: The I/O Event Indication Status Register is only available on BA revisions of the 017. (See device top mark for revision level.)

4.2 CONFIGURATION REGISTERS

EEPROM Register

Address: SELECT 0AH
Name: PCMCIA Configuration Option Register CCR0
Type: Write/Read

Bit	Configuration	Comments
Bits 5–0	Configuration Index	Card configuration chosen by the system.
Bit 6	Level Request	Level mode interrupts are selected when this bit is set to 1. Pulse mode interrupts are selected when this bit is set to 0. Also see Table 3–2.
Bit 7	SRESET	Setting this bit to 1 places the card in the reset state.

EEPROM Register

Address: SELECT 0BH
Name: PCMCIA Card Status Register CCR1
Type: Write/Read

Bit	Configuration	Comments
Bit 0	Reserved	Must be 0.
Bit 1	Interrupt	This bit represents the state of the Interrupt request signal.
Bit 2	Power Down	The card enters the power down state when this bit is set to 1. Also see Register 2BH.
Bit 3	Audio	Set this bit to 1 for audio information.
Bit 4	Reserved	Must be 0.
Bit 5	IOIS8	System can only provide I/O cycles with an 8-bit D7-D0 data path.
Bit 6	SIGCHG	This bit is set and reset by the host to allow a state change from the status register. Also see Register 1FH.
Bit 7	Changed	

EEPROM Register

Address: SELECT 0CH
Name: PCMCIA Pin Replacement Register CCR2
Type: Write/Read

Bit	Configuration	Comments
Bit 0	RWPROT	Write Protect switch.
Bit 1	RRDY//BSY	When read, this bit represents the internal state of the RRDY//BSY signal. When written, this bit acts as a mark for writing the corresponding bit CRDY//BSY.
Bit 2	RBVD2	When read, this bit represents the internal state of the Battery Voltage detection circuits on cards which contain a battery. This signal represents the values on PCMCIA pin BVD2. Also see Register 2CH.
Bit 3	RBVD1	When read, this bit represents the internal state of the Battery Voltage detection circuits on cards which contain a battery. This signal represents the values on PCMCIA pin BVD1. Also see Register 2CH.
Bit 4*	CWPROT	This bit is set to 1 when RWPROT changes state.
Bit 5*	CRDY//BSY	This bit is set to 1 when the bit RRDY//BSY changes state.
Bit 6*	CBVD2	This bit is set to 1 when the corresponding bit RBVD2 changes state.
Bit 7*	CBVD1	This bit is set to 1 when the corresponding bit RBVD1 changes state.

Note: * When this register is read, these four bits are reset.

EEPROM Register

Address: SELECT 0DH
Name: PCMCIA Socket and Copy Register CCR3
Type: Write/Read

Bit	Configuration	Comments
Bits 3–0	Socket Number	This field indicates to the card that it is located in the nth socket. The first socket is numbered 0. This permits cards designed to share a common set of I/O ports to do so while remaining uniquely identifiable.
Bits 5–4	Copy Number	Cards which indicate in their CIS that they support more than one copy of identically configured cards, should have a copy number (0 to MAX twin cards, MAX = n – 1) written back to the socket and copy register.
Bit 7	Reserved	

4.2 CONFIGURATION REGISTERS (Continued)

EEPROM Register

Address: SELECT 1FH
Name: PCMCIA I/O Event Indication CCR4
Type: Read/Write

Bit Placement	Bit Name	Description
Bit 7	RSVDEVT3	This bit is set by the input pin EXTP_STSCHG/RES2. When this bit is set and the PIEnab bit is set to 1, the changed bit in the Card configuration and status register will also be set to 1.
Bit 6	RSVDEVT2	This bit is set by the input pin ATA_DATA8/RES1. When this bit is set and the PIEnab bit is set to 1, the changed bit in the Card configuration and status register will also be set to 1.
Bit 5	PIEvt	This bit is latched to a 1 by the card after the receipt of a validated incoming packet over an RF channel. The source of this signal is ATA_DATA9/PACK_IN. When this bit is set to 1 and the PIEnab bit is set to 1, the changed bit in the Card configuration and status register will also be set to 1. And, if the SIGCHG bit in the card configuration status register has also been set by the host, then the STSCHG pin (pin 63) will go Low. The host writing a 1 to this bit will clear it to 0. Writing a 0 to this bit will have no effect.
Bit 4	RIEvt	This bit is latched to a 1 by the card after the receipt of a 1 on the /ATAPDIAG/ATA_BHE/RING-IN signal. When this bit is set to 1 and the RIEnab bit is set to 1, the changed bit in the Card configuration and status register will also be set to 1. And, if the SIGCHG bit in the card configuration status register has also been set by the host, then the STSCHG pin (pin 63) will go Low. The host writing a 1 to this bit will clear it to 0. Writing a 0 to this bit will have no effect.
Bit 3	RSVDENAB3	Setting this bit enables the Changed bit in the card configuration and status register to be set when the RSVDEVT3 bit is set. When this bit is cleared, this feature is disabled.
Bit 2	RSVDENAB2	Setting this bit enables the Changed bit in the card configuration and status register to be set when the RSVDEVT2 bit is set. When this bit is cleared, this feature is disabled.
Bit 1	PIENAB	Setting this bit enables the changed bit in the Card configuration and status register to be set when the PIEvt bit is set. When this bit is cleared, this feature is disabled.
Bit 0	RIENAB	Setting this bit enables the changed bit in the Card configuration and status register to be set when the RIEvt bit is set. When this bit is cleared, this feature is disabled.