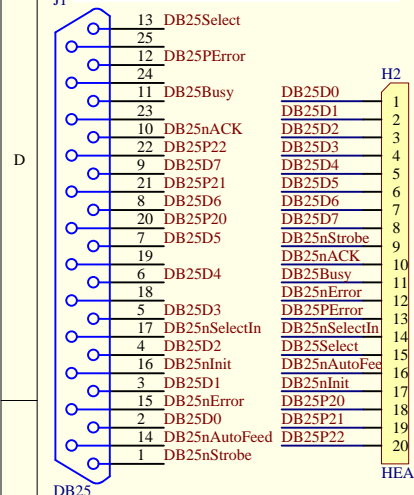
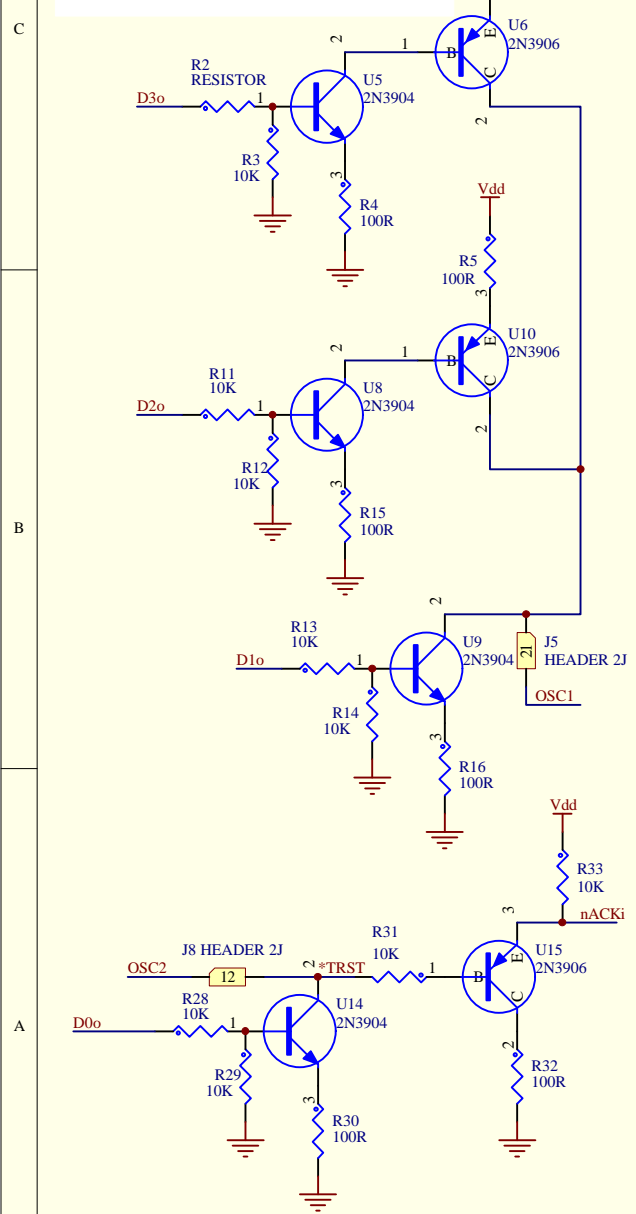


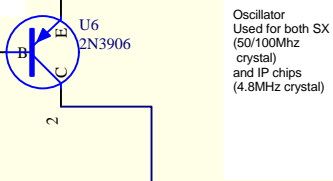
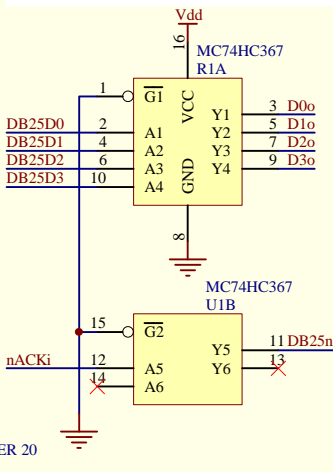
A DB25 to 0.1 Inch header adapter. Placed at the right edge past the width of the SIMM to be broken off.



Absolute Minimum SX18/28 (and I hope SX48/52) device programmer.
Also needs the MC74HC367 above and the 12V supply.
From the 3Chip crew at <http://members.rofl.com/dturner>

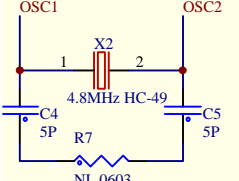
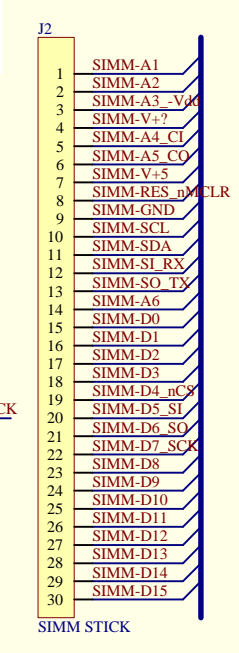
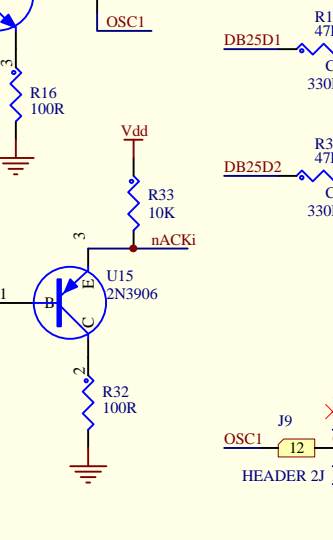


Parallel Port Buffer.
Needed for the Minimal SX programmer below left.
Would be nice to make this a part of the DB25 adapter area.



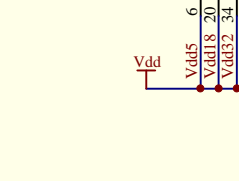
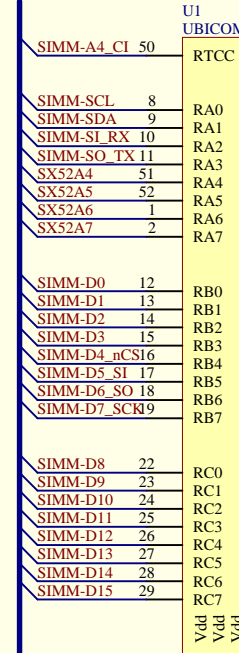
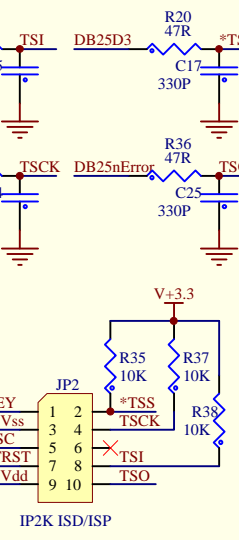
Reset Used for both the SX and IP chips.

Parallel port 'dongle' as described by Ubicom's Stephen Holland.
This allows both programming and debugging of the IP2022 via the Red Hat GNUPro tool chain.



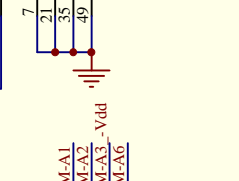
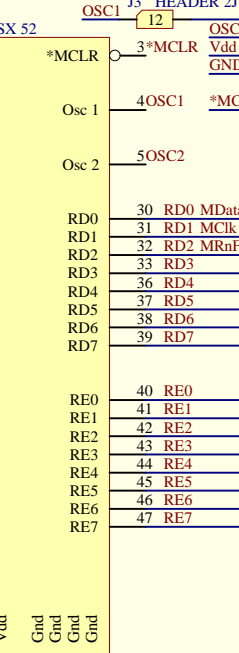
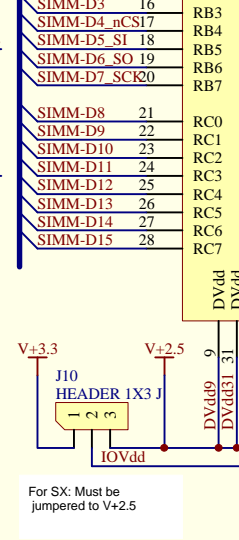
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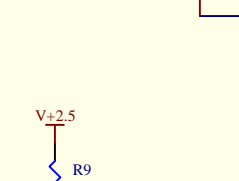
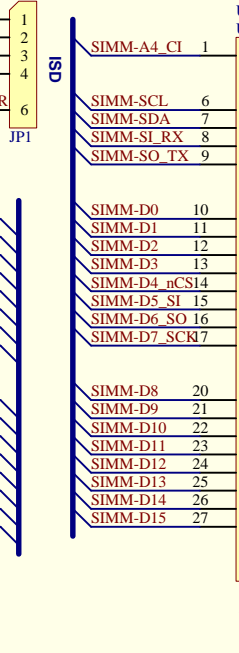
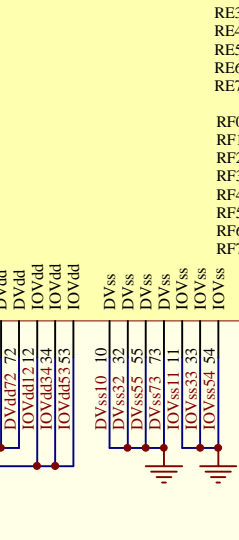
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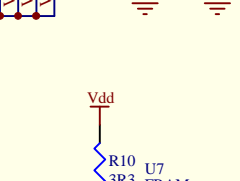
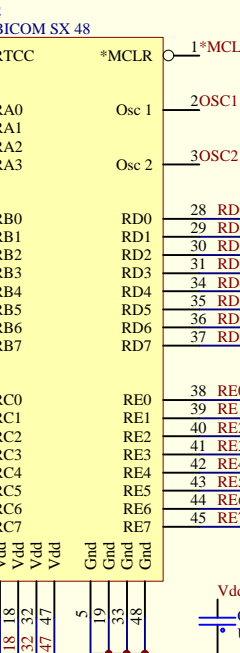
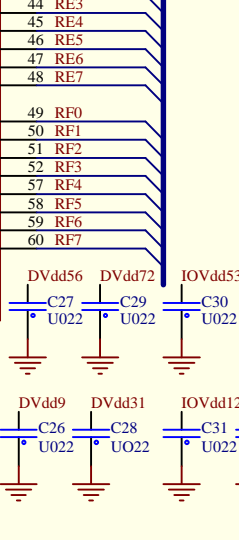
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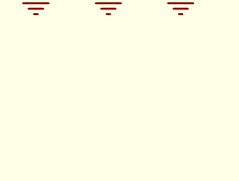
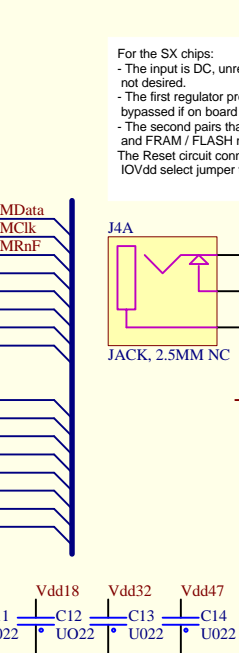
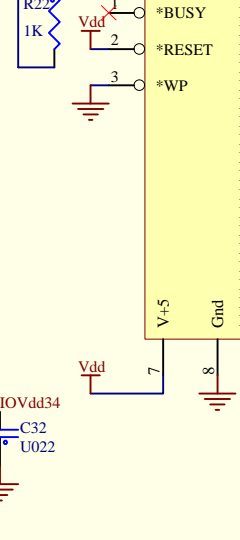
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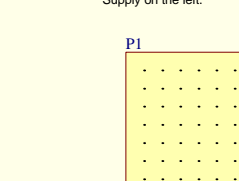
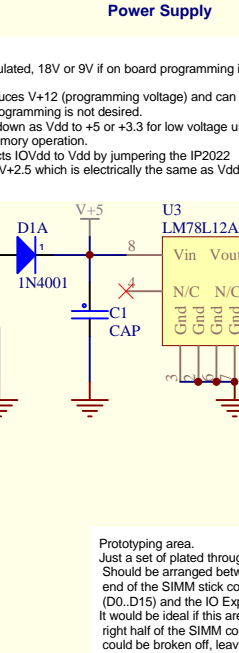
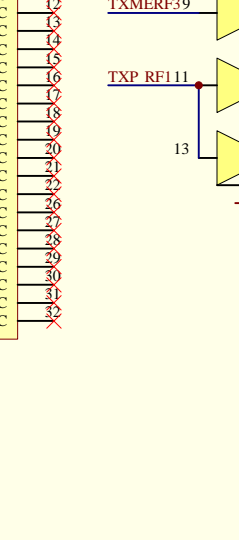
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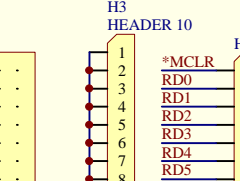
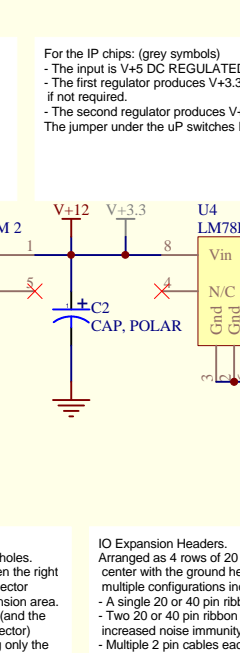
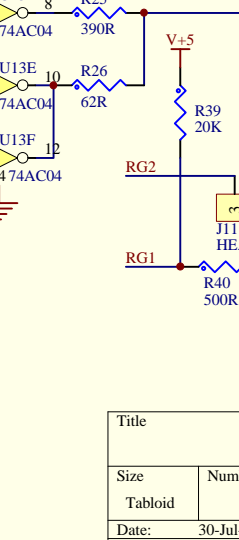
Reset Used for both the SX and IP chips.

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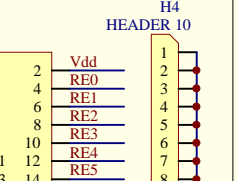
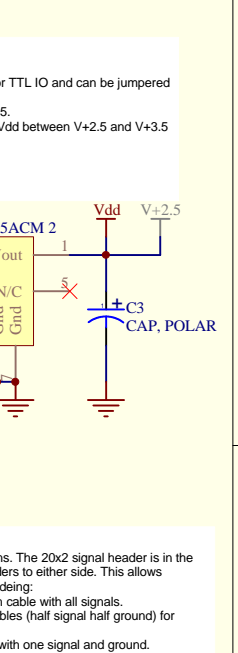
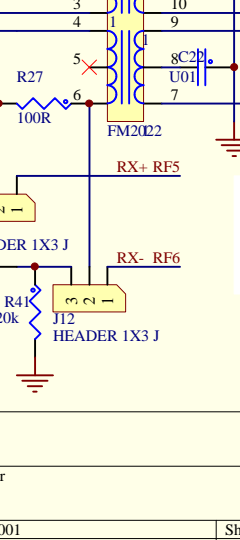
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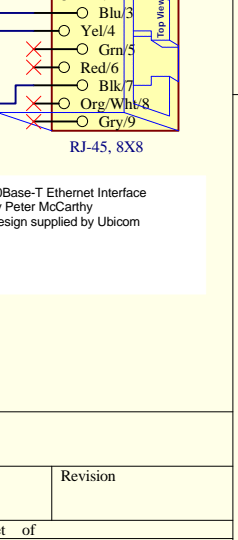
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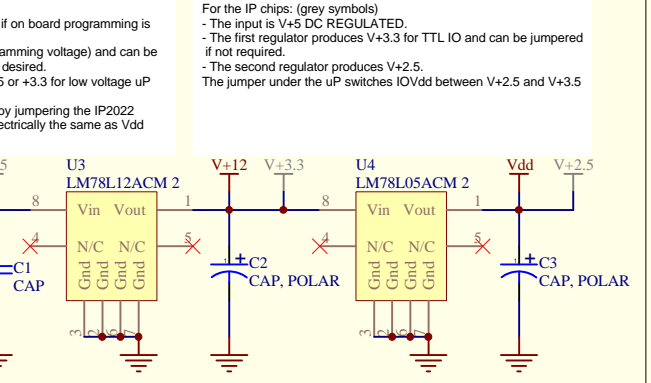


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Power Supply

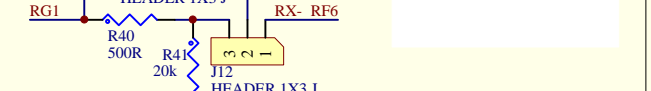
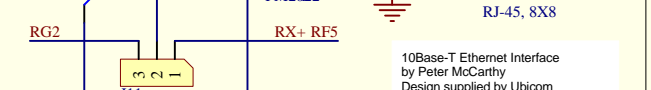
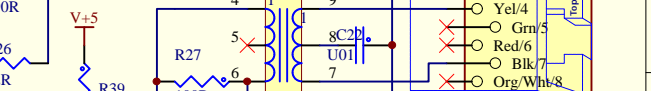
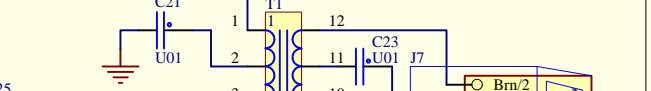
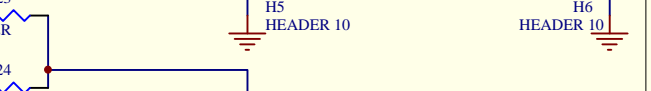
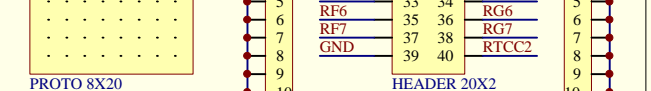
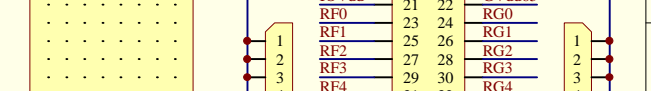
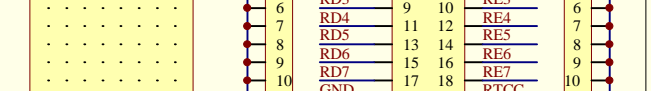


For the SX chips:
- The input is DC, unregulated, 18V or 9V if on board programming is not desired.
- The first regulator produces V+12 (programming voltage) and can be bypassed if on board programming is not desired.
- The second regulator produces V+2.5.
- The second regulator produces V+2.5.
- The Reset circuit connects IOVdd to Vdd by jumpering the IP2022 IOVdd select jumper to V+2.5 which is electrically the same as Vdd

For the IP chips: (grey symbols)
- The input is V+5 DC REGULATED.
- The first regulator produces V+3.3 for TTL IO and can be jumpered if not required.
- The second regulator produces V+2.5.
- The jumper under the uP switches IOVdd between V+2.5 and V+3.5

Prototyping area.
Just a set of plated through holes.
Should be arranged between the right end of the SIMM stick connector (D0-D15) and the IO Expansion area.
It would be ideal if this area (and the right half of the SIMM connector) could be broken off, leaving only the core components and the Power Supply on the left.

IO Expansion Headers.
Arranged as four rows of 20 pins. The 20x2 signal header is in the center with the ground headers to either side. This allows multiple configurations including:
- A single 20 or 40 pin ribbon cable with all signals.
- Two 20 or 40 pin ribbon cables (half signal half ground) for increased noise immunity
- Multiple 2 pin cables each with one signal and ground. Should be placed 0.1 inch from top edge of board.



Title	Number	Revision
Size		
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